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EXAMINER	
ELPENORD, CANDAL	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,674	VARMA, ANUJAN	
	Examiner	Art Unit	
	CANDAL ELPENORD	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *14-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 27-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :14 January 2005, 02 November 2007, March 03, 2008, April 28, 2008.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-13, 27-36 have been considered but are moot in view of the new ground(s) of rejection.

2. Claims 1, 27, 34 have been amended and claims 19-26 have been cancelled.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claims 1, 7-9, 11-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,999,413 B2) in view of Miles et al (US 6,665,495 B1).

Regarding claim 1, Moriwaki '413 discloses a switching device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27) comprising a

segmentation unit (fig. 1, fig. 3 to fig. 4, see "Block Generating" where variable length packets are divided, col. 7, lines 7-27) to receive data packets of variable size from external sources (fig. 1, see variable length packets being received at Input Line 40-1 to 40-n, col. 6, lines 35-41), to divide packets having a length greater than a maximum segment length into a plurality of segments (fig. 4, see, combining of incoming packets, recited in col. 7, lines 22-26, "variable lengths are divided and stored in a queue", recited in col. 7, lines 7-20-since the packets being fragmenting are of variable length, therefore their size vary), and to store the data packets as segments (fig. 4, see, combining of incoming packets, recited in col. 7, lines 22-26, "variable length packets are divided and stored in a queue", recited in col. 7, lines 7-20); wherein each data packet includes one or more segments (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26), each segment has a length that is less than or equal to the maximum segment length, and each segment identifies whether additional segments are included in the associated data packet the data packets received having a length greater than a maximum segment length are divided into multiple segments; a plurality of queues to store the segments ("stored variable length packet in block generating queue (VOQ 23-1, 23-n), recited in col. 7, lines 11-17, wherein the queues (fig. 1, fig. 3, see Virtual output Queues 23-1 to 23-n) are associated with destinations (fig. 1, Line Interfaces 20-1, 20-n, Output Line 50-1, 50-n, recited in col. 6, lines 17-27); a scheduler (fig. 1, Scheduler 11, col. 6, lines 32-41), a state monitor to track complete packets contained within the plurality of egress queues ("detecting boundaries of variable length packets", recited in col. 10, lines 8-24); and a

reassembly unit to combine the segments making up a complete packet together to generate the packet ("packets regenerating so variable length packet can be obtained form fixed length blocks stored in the queue buffer", recited in col. 10, lines 8-17, fig. 4, Packet Regenerating); and to transmit the packets to external sources (fig. 1, Egress Lines 20-1 and 20-n) to generate a schedule including a data path from at least one queue("the scheduler decides the optimum input/output connections by schedule algorithm", recited in col. 9, lines5-13) to an associated destination (fig. 1, Line Interfaces 20-1, 20-n, Output Line 50-1, 50-n, recited in col. 6, lines 17-27).

Moriwaki '413 discloses all the claimed limitations with the exception of being silent with respect to claimed features: **regarding claim 1**, a framer to aggregate a plurality of segments to form a frame, wherein the frame has a maximum frame length, wherein the segments are retrieved from the at least one queue, and wherein the frame may contain segments associated with different data packets; a transmitter to transmit the frame to the associated destination, wherein the segments within the frame are transmitted together; and a switch fabric to provide a configurable connection between the external a plurality of sources and external a plurality of destinations, wherein said switch fabric is configured by said scheduler, and wherein said switch fabric transmits frames from at least a subset of the external plurality of sources to at least a subset of the external plurality of destinations during a schedule cycle.

Regarding claim 7, the device, wherein said plurality of queues include one or more queues per destination based on priorities associated with the destinations.

Regarding claim 8, the device, wherein said framer forms the flame by

aggregating segments from some subset of the one or more associated queues.

Regarding claim 9, the device, wherein said framer forms the flame by aggregating complete segments.

Regarding claim 11, **the** device, wherein said transmitter transmits the segments making up a particular data packet in order.

Regarding claim 12, the device, wherein said transmitter interleaves segments associated with different data packets.

Regarding claim 13, the device, further comprising a striper to stripe the frame across a plurality of channels.

Miles '495 from the same field of endeavor discloses the above claimed features:

Regarding claim 1, a framer (fig. 4,Ingress Edge unit 60, aggregates of data packets to form a super packet, col. 7, lines 23-33, see, "aggregating of data packets to form a super packet", col. 3, lines 67 to col. 4, lines 7, fig. 12a, see Supper Packet Processor) to aggregate a plurality of segments (see, super packet contains data packets, col. 7, lines 38-41) to form a frame (see, aggregates of data packets to form a super packets, col. 7, lines 23-33, see, "aggregating of data packets to form a super packet", col. 3, lines 67 to col. 4, lines 7), wherein the frame has a maximum frame length, wherein the segments are retrieved from the at least one queue (fig. 13, Queue 114 (memory device), col. 20, lines 5-11), and wherein the frame (see "aggregating of data packets to form a super packet", col. 3, lines 67 to col. 4, lines 7) may contain segments associated with different data packets (fig. 7, see super packet containing plurality of variable length packets, col. 13, lines 3-11); a transmitter (fig. 4 to fig. 5, see

super packet being sent to egress side via the super packet links, col. 9, lines 34-46) to transmit the frame to the associated destination (fig. 4 to fig. 5, see super packet being sent to egress side via the super packet links, col. 9, lines 34-46), wherein the segments within the frame are transmitted together; and a switch fabric (fig. 4 to fig. 5, Optical Switch Fabric 70, col. 8, lines 39-52) to provide a configurable connection (see, switching of input to output by the switching fabric, col. 13, lines 1-15) between the external a plurality of sources (fig. 4, Input/output line interfaces 28, col. 7, lines 48-57) and external a plurality of destinations (fig. 4, see output line interfaces 28 connecting to Egress Edge Units, col. 7, lines 48-57), wherein said switch fabric (fig. 4 to fig. 5, see Optical Switch Fabric 70, col. 8, lines 39-52) is configured by said scheduler (fig. 5, Super Packet Scheduler 42, col. 8, lines 43-58), and wherein said switch fabric (fig. 4 to fig. 5, Optical Switch Fabric 70, col. 8, lines 39-52) transmits frames (see, the ingress edge unit aggregate plurality (4 data packets in a super packet) intended for the egress edge units, col. 13, lines 17-40) from at least a subset of the external plurality of sources (fig. 4, Input/output line interfaces 28, col. 7, lines 48-57) to at least a subset of the external plurality of destinations (fig. 4, see output line interfaces 28 connecting to Egress Edge Units, col. 7, lines 48-57) during a schedule cycle (see, "computing of a scheduling pattern for super packet based on traffic characteristics", col. 3, lines 23-31, see, pattern of sending super packets intended for particular destinations, col. 16, lines 11-60).

Regarding claim 7, wherein said plurality of queues include one or more queues (fig. 14, Buffers/queues 130, col. 22, lines 44-50) per destination (see, "queues based

on egress destinations", col. 22, lines 44-50) based on priorities ("quality of service requirements such voice data, video data, col. 20, lines 11-21) associated with the destinations (see, examining header of incoming data packets to determine destination, col. 20, lines 11-21).

Regarding claim 8, wherein said framer (fig. 4,Ingress Edge unit 60, aggregates of data packets to form a super packet, col. 7, lines 23-33, see, "aggregating of data packets to form a super packet", col. 3, lines 67 to col. 4, lines 7, fig. 12a, see Supper Packet Processor) forms the flame by aggregating segments (see, "aggregating of data packets to form a super packet", col. 3, lines 67 to col. 4, lines 7, from some subset of the one or more associated queues (fig. 14, see, building of super packets from the super packet ingress queue, col. 21, lines 44-64).

Regarding claim 9, wherein said framer forms the flame (fig. 4,Ingress Edge unit 60, aggregates of data packets to form a super packet, col. 7, lines 23-33, see, "aggregating of data packets to form a super packet", col. 3, lines 67 to col. 4, lines 7, fig. 12a, see Supper Packet Processor) by aggregating complete segments (see, multiplexing of partial super packet to form the super packet, col. 21, lines 44-64).

Regarding claim 11, the device, wherein said transmitter (fig. 9, edge ingress unit transmits packets to the switching fabric which then transmits the packets at particular time slot to egress edge unit) transmits the segments making up a particular data packet in order (delivery and sending of super packets based on time, col. 16, lines47-56).

Regarding claim 12, the device, wherein said transmitter (fig. 9, edge ingress unit transmits packets to the switching fabric which then transmits the packets at particular time slot to egress edge unit)r interleaves segments associated with different data packets (see, multiplexed of partial super packets for subsequent transmission to the transmit controller, col. 21, lines 36 to col. 22, lines 17).

Regarding claim 11, the device, wherein said transmitter (fig. 9, edge ingress unit transmits packets to the switching fabric which then transmits the packets at particular time slot to egress edge unit) transmits the segments making up a particular data packet in order (delivery and sending of super packets based on time, col. 16, lines47-56).

Regarding claim 13, further comprising a striper (fig. 14, see Super Packet Transmit Controller 126, col. 22, lines 7-17) to stripe the frame (see, transmit over 16 lambdas, col. 22, lines 7-17) across a plurality of channels (see, delivering of super packets over DWDM optical fiber across multiple lambda, col. 19, lines 23-27).

In view of the above, having the packet switching apparatus for segmenting variable packets into blocks of Moriwaki '413, the system and method for providing non-blocking routing optical where optical data packets are aggregated into super packets of Miles '495, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki '413 by using features of Miles in order to aggregate plurality of data packets into a super packet to optimize throughput as suggested in col. 3, lines 67 to col. 4, lines 7.

6. **Claims 27-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,699,413 B2) in view of Miles et al (US 6,665,495 B1).

Regarding claim 27, Moriwaki et al. disclose a store and forward device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27) comprising a plurality of Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) to receive data from ("receiving of variable length packets", recited in col. 6, lines 23-29) and transmit data ("routing processing of variable length packets", recited in col. 6, lines 23-29) to external sources (fig. 1, Line Interfaces 20-1, 20-n, recited in col. 6, lines 17-25), wherein the plurality of Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) include a segmentation unit (fig. 1, fig. 3 to fig. 4, see "Block Generating" where variable length packets are divided, col. 7, lines 7-27) to receive data packets of variable size from external sources (fig. 1, see variable length packets being received at Input Line 40-1 to 40-n, col. 6, lines 35-41), to divide packets having a length greater than a maximum segment length into a plurality of segments (fig. 4, see, combining of incoming packets, recited in col. 7, lines 22-26, "variable lengths are divided and stored in a queue", recited in col. 7, lines 7-20-since the packets being fragmenting are of variable length, therefore their sizes vary), and to store the data packets as segments (fig. 4, see, combining of incoming packets, recited in col. 7, lines 22-26, "variable length packets are divided and stored in a queue", recited in col. 7, lines 7-20); wherein each data packet includes one or more segments (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26), each segment has

a length that is less than or equal to the maximum segment length, and each segment identifies whether additional segments are included in the associated data packet (fig, 3 to fig. 4, see Variable Length packets E, D, C, A and associated Blocks 3, Block 2 and Block 1) ; a plurality of queues to store the segments ("stored variable length packet in block generating queue (VOQ 23-1, 23-n), recited in col. 7, lines 11-17, wherein the queues (fig. 1, fig. 3, see Virtual output Queues 23-1 to 23-n) are associated with destinations (fig. 1, Line Interfaces 20-1, 20-n, Output Line 50-1, 50-n, recited in col. 6, lines 17-27); a state monitor to track complete packets contained within the plurality of egress queues ("detecting boundaries of variable length packets", recited in col. 10, lines 8-24); and a reassembly unit to combine the segments making up a complete packet together to generate the packet ("packets regenerating so variable length packet can be obtained form fixed length blocks stored in the queue buffer", recited in col. 10, lines 8-17, fig. 4, Packet Regenerating); and to transmit the packets to external sources (fig. 1, Egress Lines 20-1 and 20-n).

Regarding claim 28, the device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), wherein said backplane (fig. 1, fig. 11, "crossbar switching planes 10-1 to 10-5", recited in col. 9, lines 14-21) also connects said plurality of Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) to said scheduler (fig. 1, Scheduler 11, recited in col. 6, lines 29-41).

Regarding claim 29, the device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), wherein said backplane (fig. 1, fig. 11,

"crossbar switching planes 10-1 to 10-5", recited in col. 9, lines 14-21) uses same channels (fig. 1, Connection Links 41-1-x to 41-5-x, recited in col. 6, lines 35-41) to connect said Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) to said switching matrix (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41); and to said scheduler (fig. 1, Scheduler 11, recited in col. 6, lines 29-41).

Regarding claim 30, the device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), wherein said backplane (fig. 1, fig. 11, "crossbar switching planes 10-1 to 10-5", recited in col. 9, lines 14-21) provides a logical separation of data path ("allocation of time slot corresponding to n crossbar switches", recited in col. 4, lines 9-15) between said Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) and said switching matrix (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41) and scheduling path between said Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) and said scheduler (fig. 1, Scheduler 11, recited in col. 6, lines 29-41).

Regarding claim 32, the device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), wherein the backplane (fig. 1, fig. 11, "crossbar switching planes 10-1 to 10-5", recited in col. 9, lines 14-21) is optical (fig. 2B, SONET framing structure, recited in col. 10, lines 25-40);

Regarding claim 33, the device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), wherein the switching matrix (fig. 1, Crossbar

Switch (nxn)10, recited in col. 6, lines 17-41) is optical (fig. 2B, SONET framing structure, recited in col. 10, lines 25-40).

Moriwaki '479 discloses all the claimed limitations with the exception of being silent with respect to claimed features:

Regarding claim 27, a framer to aggregate a plurality of segments associated with a destination to form a frame to be transmitted, wherein the frame may contain segments associated with different data packets; a deframer to receive a transmitted frame and to extract segments making up the frame therefrom; a plurality of egress queues to store the extracted segments based on destinations; a switching matrix to provide selective connectivity between said Ethernet cards to transmit; frames therebetween a backplane consisting of a plurality of channels to connect said plurality of Ethernet cards to said switching matrix; and a scheduler to select connectivity between Ethernet cards and to configure said switching matrix accordingly.

Regarding claim 31, wherein the maximum frame size is selected based on at least some subset of configuration time of data path, scheduling time for scheduler, and complexity of scheduling algorithms.

Miles '495 from the same field of endeavor discloses the above claimed features:

Regarding claim 27, a framer (fig. 4,Ingress Edge unit 60, aggregates of data packets to form a super packet, col. 7, lines 23-33, see, "aggregating of data packets to form a super packet", col. 3, lines 67 to col. 4, lines 7, fig. 12a, see Supper Packet Processor, see, construction of super packet, col. 22, lines 41-50) to aggregate a

plurality of segments (see, super packet contains data packets, col. 7, lines 38-41) associated with a destination (see, aggregation of optical data intended for destination, col. 13, lines 17-22) to form a frame (see, aggregates of data packets to form a super packets, col. 7, lines 23-33, see, "aggregating of data packets to form a super packet", col. 3, lines 67 to col. 4, lines 7), wherein the frame may contain segments associated with different data packets (see, multiplexed of partial super packets to form super packets, col. 21, lines 36-50); a deframer (fig. 12b, Egress Edge Unit receiving the super packets form the Ingress Edge unit to deconstruct/de-aggregate the super packets, col. 19, lines 36-51) to receive a transmitted frame and to extract segments making up the frame therefrom (fig. 12b, Egress Edge Unit receiving the super packets form the Ingress Edge unit to deconstruct/de-aggregate the super packets, col. 19, lines 36-51); a plurality of egress queues to store the extracted segments based on destinations (fig. 15, Super packet Egress Queue 138, see deconstruction of the super packets and then place the super packet in the queues, col. 23, lines 12-20); a switching matrix (fig. 4 to fig. 5, see Optical Switch Fabric 70, col. 8, lines 39-52) to provide selective connectivity between said Ethernet cards (fig. 4, Input/Output lines-Ethernet Port cards, col. 7, lines 48-57) to transmit frames therebetween; a backplane (fig. 4, see back of the optical core fabric which includes a plurality of optical data links connecting to ingress and egress edge units, col. 7, lines 48-57) consisting of a plurality of channels (fig. 4, see back of the optical core fabric which includes a plurality of optical data links connecting to ingress and egress edge units, col. 7, lines 48-57) to connect said plurality of Ethernet cards (fig. 4, Input/Output lines-Ethernet Port cards, col. 7,

lines 48-57) to said switching matrix (fig. 4 to fig. 5, Optical Switch Fabric 70, col. 8, lines 39-52); and a scheduler (fig. 4 in combination with fig. 5, Super Packet Scheduler 42, col. 8, lines 43-58) to select connectivity (see, switching of input to output by the switching fabric, col. 13, lines 1-15) between Ethernet cards (fig. 4, Input/Output lines-Ethernet Port cards, col. 7, lines 48-57) and to configure said switching matrix accordingly (see, "computing of a scheduling pattern for super packet based on traffic characteristics", col. 3, lines 23-31, see, pattern of sending super packets intended for particular destinations, col. 16, lines 11-60, see coordinating of switching, col. 43-57).

Regarding claim 31, wherein the maximum frame size ("super packets", recited in col. 7, lines 27-33) is selected based on at least some subset of configuration time ("selected time and scheduling pattern", recited in col. 36-48) of data path ("placing of packet on the ingress links a time slots", recited in col. 14, lines 32-55), scheduling time for scheduler ("the controller schedules super packets based on scheduled algorithm", recited in col. 3, lines 29-31), and complexity of scheduling algorithms ("contention among the plurality of super packets in the transmission between the optical switch fabric and the egress units", recited in col. 3, lines 15-23).

In view of the above, having the packet switching apparatus for segmenting variable packets into blocks of Moriwaki '413, the system and method for providing non-blocking routing optical where optical data packets are aggregated into super packets of Miles '495, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki '413 by using features of Miles in

order to aggregate plurality of data packets into a super packet to optimize throughput as suggested in col. 3, lines 67 to col. 4, lines 7.

Regarding claim 34, Moriwaki et al. discloses a store and forward device (fig. 1, Packet Communication Apparatus, recited in col. 6, lines 17-27) comprising a plurality of ingress interface modules (fig. 1, Line I/F #1, Line I/F #n, recited in col. 6, lines 17-27), wherein each interface module include a segmentation unit to receive packets of variable size ("incoming variable length packets", recited in col. 6, lines 17-27) from external sources (fig. 1, Input Line -40-1, Input Line 40-n), a segmentation unit (fig. 1, fig. 3 to fig. 4, see "Block Generating" where variable length packets are divided, col. 7, lines 7-27) to receive data packets of variable size from external sources (fig. 1, see variable length packets being received at Input Line 40-1 to 40-n, col. 6, lines 35-41), to divide packets having a length greater than a maximum segment length into a plurality of segments (fig. 4, see, combining of incoming packets, recited in col. 7, lines 22-26, "variable lengths are divided and stored in a queue", recited in col. 7, lines 7-20-since the packets being fragmenting are of variable length, therefore their sizes vary), and to store the data packets as segments (fig. 4, see, combining of incoming packets, recited in col. 7, lines 22-26, "variable length packets are divided and stored in a queue", recited in col. 7, lines 7-20); wherein each data packet includes one or more segments (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26), each segment has a length that is less than or equal to the maximum segment length, and each segment identifies whether additional segments

are included in the associated data packet (fig, 3 to fig. 4, see Variable Length packets E, D, C, A and associated Blocks 3, Block 2 and Block 1); a plurality of queues to store the segments ("stored variable length packet in block generating queue (VOQ 23-1, 23-n), recited in col. 7, lines 11-17, wherein the queues (fig. 1, fig. 3, see Virtual output Queues 23-1 to 23-n) are associated with destinations (fig. 1, Line Interfaces 20-1, 20-n, Output Line 50-1, 50-n, recited in col. 6, lines 17-27); a state monitor to track complete packets contained within the plurality of egress queues ("detecting boundaries of variable length packets", recited in col. 10, lines 8-24); and a reassembly unit to combine the segments making up a complete packet together to generate the packet ("packets regenerating so variable length packet can be obtained form fixed length blocks stored in the queue buffer", recited in col. 10, lines 8-17, fig. 4, Packet Regenerating); and to transmit the packets to external sources (fig. 1, Egress Lines 20-1 and 20-n).

Moriwaki '413 discloses all the claimed limitations with the exception of being silent with respect to claimed features: **regarding claim 34,** a framer to aggregate a plurality of segments associated with a destination to form a frame to be transmitted, wherein the frame may contain segments associated with different data packets; a deframer to receive a transmitted frame and to extract segments making up the frame therefrom; a plurality of egress interface modules, wherein each egress interface modules, a plurality of queues to store the extracted segments based on destinations; a switching matrix to provide selective connectivity between said Ethernet cards to transmit frames therebetween a backplane consisting of a plurality of channels to

connect said plurality of Ethernet cards to said switching matrix; and a scheduler to select connectivity between Ethernet cards and to configure said switching matrix accordingly.

Miles '495 from the same field of endeavor discloses the above claimed features;

Regarding claim 34, a framer (fig. 4,Ingress Edge unit 60, aggregates of data packets to form a super packet, col. 7, lines 23-33, see, "aggregating of data packets to form a super packet", col. 3, lines 67 to col. 4, lines 7, fig. 12a, see Supper Packet Processor, see, construction of super packet, col. 22, lines 41-50) to aggregate a plurality of segments (see, super packet contains data packets, col. 7, lines 38-41) associated with a destination (see, aggregation of optical data intended for destination, col. 13, lines 17-22) to form a frame (see, aggregates of data packets to form a super packets, col. 7, lines 23-33, see, "aggregating of data packets to form a super packet", col. 3, lines 67 to col. 4, lines 7), wherein the frame may contain segments associated with different data packets (see, multiplexed of partial super packets to form super packets, col. 21, lines 36-50); a plurality of egress interface modules (fig. 4 in combination with the fig. 12a, Egress Edge Units E16, col. 8, lines 20-29) wherein each egress interface module (fig. 4, Egress Edge Unit 1) includes, a deframer (fig. 12b, Egress Edge Unit receiving the super packets form the Ingress Edge unit to deconstruct/de-aggregate the super packets, col. 19, lines 36-51) to receive a transmitted frame and to extract segments making up the frame therefrom (fig. 12b, Egress Edge Unit receiving the super packets form the Ingress Edge unit to deconstruct/de-aggregate the super packets, col. 19, lines 36-51); a plurality of egress

queues to store the extracted segments based on destinations (fig. 15, Super packet Egress Queue 138, see deconstruction of the super packets and then place the super packet in the queues, col. 23, lines 12-20); a switching matrix (fig. 4 to fig. 5, see Optical Switch Fabric 70, col. 8, lines 39-52) to provide selective connectivity between said Ethernet cards (fig. 4, Input/Output lines-Ethernet Port cards, col. 7, lines 48-57) to transmit frames therebetween; a backplane (fig. 4, see back of the optical core fabric which includes a plurality of optical data links connecting to ingress and egress edge units, col. 7, lines 48-57) consisting of a plurality of channels (fig. 4, see back of the optical core fabric which includes a plurality of optical data links connecting to ingress and egress edge units, col. 7, lines 48-57) to connect said plurality of ingress interface modules and the plurality of egress interface modules (fig. 4, Input/Output lines-Ethernet Port cards, col. 7, lines 48-57, see Ingress and Egress Edge Units) to said switching matrix (fig. 4 to fig. 5, Optical Switch Fabric 70, col. 8, lines 39-52); and a scheduler (fig. 4 in combination with fig. 5, Super Packet Scheduler 42, col. 8, lines 43-58) to select connectivity (see, switching of input to output by the switching fabric, col. 13, lines 1-15) between the plurality of ingress interface modules and the plurality of egress interface modules (fig. 4, Input/Output lines-Ethernet Port cards, col. 7, lines 48-57, see ingress and egress edge units) and to configure said switching matrix accordingly (see, "computing of a scheduling pattern for super packet based on traffic characteristics", col. 3, lines 23-31, see, pattern of sending super packets intended for particular destinations, col. 16, lines 11-60, see coordinating of switching, col. 43-57).

In view of the above, having the packet switching apparatus for segmenting variable packets into blocks of Moriwaki '413, the system and method for providing non-blocking routing optical where optical data packets are aggregated into super packets of Miles '495, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki '413 by using features of Miles in order to aggregate plurality of data packets into a super packet to optimize throughput as suggested in col. 3, lines 67 to col. 4, lines 7.

7. **Claims 2-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al(US 6,999, 413 B2) in view of Miles et al (US 6,665,495 B1) as applied to claim1 above, and further in view of view of Antal et al (US 7,224,703 B2).

Moriwaki '413 and Miles '495 discloses all the claimed limitations with the exception of being silent with respect to claimed features: **regarding claim 2**, wherein said segmentation unit divides the data packets having a length greater than the maximum segment length to form at least a first segment having the maximum segment length.

Regarding claim 3, wherein a last segment formed by said segmentation unit may be less than the maximum segment length.

Regarding claim 4, the device, wherein said segmentation unit identifies a final segment belonging to a particular data packet.

Regarding claim 2, wherein said segmentation unit (fig.4, Segmenter 22, recited in col.4, lines 55-63) divides the data packets having a length greater than the maximum segment length ("data packet segmented into plural segments", recited in col. 3, lines 26-35, fig. 3, "size of largest segment of a 1013 byte packet", recited in col. 2, lines 44-48) to form at least a first segment having the maximum segment length ('setting the first segment to a size larger than the maximal segment size", recited in col. 6, lines 55-62).

Regarding claim 3, wherein a last segment ("last segment", recited in col. 3, lines 39-42) formed by said segmentation unit (fig.4, Segmenter 22, recited in col.4, lines 55-63) may be less than the maximum segment length ('the last segment is the same size as the first segment whose less than the maximal segment size", recited in col.. 3, lines 33-42).

Regarding claim 4, wherein said segmentation unit (fig.4, Segmenter 22, recited in col.4, lines 55-63) identifies a final segment belonging to a particular data packet ("smaller packet making up the last packet segment", recited in col. 1, lines 62- col. 2, line 1).

In view of the above, having the packet switching apparatus for segmenting variable packets into blocks of Moriwaki '413, the system and method for providing non-blocking routing optical where optical data packets are aggregated into super packets of Miles '495, and the method and the apparatus for segmenting data packets into plural segments a maximum size of Antal '703, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki '413

with Miles by incorporating the teaching features of Antal '703. The motivation would have been to provide transmission efficiency by reducing transmission delay as suggested in col. 3, lines 18-19.

8. **Claims 5-6, 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,999,413 B2) in view of Miles et al (US 6,665,495 B1) as applied to claim 1above, and further in view of Sakamoto et al (US 6,836,479 B1).

Regarding claim 6, Miles '495 discloses wherein said scheduler matches the requests (see, "incoming traffic demand", col. 3, lines 15-26) and resolves conflicts in order to generate the schedule (see, "computing schedule pattern to avoid contention", col. 3, lines 23-31).

Moriwaki '413 and Miles '495 discloses the device and framer as discussed in above paragraph.

Moriwaki '413 and Miles '495 are silent with respect to claimed features: **regarding claim 10**, the framer pads the frame to reach the maximum frame length; **regarding claim 5**, the device wherein said scheduler generates the schedule based on requests for data packets from particular queues to be transmitted to particular destinations.

Sakamoto '479 from the same field of endeavor discloses the above claimed features:

Regarding claim 10, the framer pads the frame to reach the maximum frame length (see, inserting of padding (PAD 19) if the packets is short of the length, col. 8, lines 63-65).

Regarding claim 5, the device wherein said scheduler generates the schedule based on requests for data packets from particular queues to be transmitted to particular destinations (the scheduler transmits packets with high priority when the transmission requests, col. 6, lines 43-48)..

In view of the above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki '413 with Miles '495 by incorporating the teaching features of Sakamoto "479 in order to generate container from the queues as suggested in col. 8, lines 61-63.

9. **Claim 35** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,999,413 B2) in view Miles et al (US 6,665,495 B1) as applied to claim 34 above and further view of Dell et al (US 2002/0085578 A1).

Regarding claim 35, Moriwaki et al. discloses the device (fig. 1, Packet Communication Apparatus, recited in col. 6, lines 17-27).

Moriwaki '413 and Miles '495 disclose all the claimed limitation with the exception of being silent with regard to the following features: wherein a pipeline schedule is implemented that includes at least some subset of said ingress interface modules forming and transmitting requests to said scheduler, scheduler computing a schedule

based on the requests, said scheduler transmitting grants to associated ingress interface modules and configuring said switching matrix, and said ingress interface modules transmitting the frames in response to the grants.

However, Dell '578 from the same field of endeavor discloses: wherein a pipeline schedule (fig. 3, see, Plural Stages 1, 2,3, recited in paragraph 0051, paragraph 0014, lines 1-13) is implemented that includes at least some subset of said ingress interface modules (fig. 2, Ingress Line cards 202, recited in paragraph 0048, lines 1-6) forming and transmitting requests ("successful request", recited in paragraph 0085, lines 9-14) to said scheduler (fig. 4, Scheduler 418, recited in paragraph 0068, lines 1-6), scheduler (fig. 4, Scheduler 418, recited in paragraph 0068, lines 1-6) computing a schedule based on the requests ("computes of schedule every clock cycle by the scheduler", recited in paragraph 0112), said schedule (fig. 4, Scheduler 418, recited in paragraph 0068, lines 1-6) transmitting grants ("granted request then the Grant signal is fed", recited in paragraph 0068, lines 6-11) to associated ingress interface modules (fig. 2, Ingress Line cards 202, recited in paragraph 0048, lines 1-6) and configuring said switching matrix (fig. 2, Switching Fabric modules 201, recited in paragraph 0047, lines 1-9), and said ingress interface modules (fig. 2, Ingress Line cards 202, recited in paragraph 0048, lines 1-6) transmitting the frames ("transmitted cells to the crossbar devices", recited in paragraph 0118) in response to the grants ("granted request then the Grant signal is fed", recited in paragraph 0068, lines 6-11).

In view of the above, , it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki '413 with Miles '495 by using features as taught by Dell '578 in order to provide stage switching of network traffic from sources to a plurality of destinations and quality of service as suggested in paragraphs 0011, 0013.

10. **Claim 36** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,999,413 B2) in view Miles et al (US 6,665,495 B1) as applied to claim 34 above and further view of Tornetta et al (US 6,950,448 B2).

Regarding claim 36, Moriwaki et al. discloses the (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27) and the switching matrix, the scheduler as recited in above paragraph, align configuration changes ("adjust of the timing", recited in col. 8, lines 36-41), and maintains an uninterrupted data stream to the egress interface modules by transmitting an idle stream when no frames are being transmitted ("supply of idle block to the line interface", recited in col. 11, lines 34-45).

Moriwaki '413 and Miles '495 disclose all the claimed limitation with the exception of being silent with regard to the following features: wherein said switching matrix extracts a clock from frames received, re-times the frames to a common internal clock domain, aligns any configuration changes provided by said scheduler to the boundaries

of the frames, and maintains an uninterrupted data stream to the egress interface modules by transmitting an idle stream when no frames are being transmitted.

However, Tornetta '448 from the same field of endeavor discloses the above claimed features:

Regarding claim 36, wherein said switching matrix (fig. 4, Switching Matrix 15, extracts a clock from frames received ("generates of serial clock", recited in col. 5, lines 55-59), re-times the frames to a common internal clock domain ("receiver use of transition to phase align recovered clock with the data", recited in col. 5, lines 60-64).

In view of the above, , it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki '413 with Miles '495 by using features as taught by Tornetta '448 in order to extract/recover clock signals from the received frames as suggested in col. 5, lines 9-25 for motivation.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Calvignac et al (US 2002/0176429).

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CANDAL ELPENORD whose telephone number is (571)270-3123. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Bin Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Candal Elpenord/
Examiner, Art Unit 2616

/Kwang B. Yao/
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